

**NEW UTILITY PATENT APPLICATION
TRANSMITTAL***(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))*Docket No.
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submission**TO THE ASSISTANT COMMISSIONER FOR PATENTS****Box Patent Application
Washington, D.C. 20231**

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

**METHOD AND MATERIAL FOR REMOVING ETCH RESIDUE FROM HIGH ASPECT RATIO
CONTACT SURFACES**

and invented by:

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IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

- ☐ Continuation ☐ Divisional
- ☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 31 pages(s) and including the following:
 - a. ☒ Descriptive title of the invention
 - b. ☐ Cross references to related applications *(if applicable)*
 - c. ☐ Statement regarding Federally-sponsored research/development *(if applicable)*
 - d. ☐ Reference to microfiche appendix *(if applicable)*
 - e. ☒ Background of the invention
 - f. ☒ Brief summary of the invention
 - g. ☒ Brief description of the drawings *(if drawings filed)*
 - h. ☒ Detailed description
 - i. ☒ Claims as classified below
 - j. ☒ Abstract of the disclosure

Application Elements (continued)

3. ☒ Drawing(s) (when necessary as prescribed by 35 U.S.C. 113)
☒ Formal ☐ Informal Number of sheets: 6
4. ☒ Oath or Declaration
 a. ☒ Newly executed (original or copy) ☐ Unexecuted
 b. ☐ Copy from a prior application (37 C.F.R. 1.63(d) (for continuation/divisional applications only)
 c. ☐ With Power of Attorney ☒ Without Power of Attorney
5. ☐ Incorporation by reference (usable if Box 4b is checked)
 The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer program in microfiche
7. ☐ Genetic sequence submission (if applicable, all must be included)
 a. ☐ Paper copy
 b. ☐ Computer readable copy
 c. ☐ Statement verifying identical paper and computer readable copies

Accompanying Application

8. ☒ Assignment papers (cover sheet & document(s))
9. ☐ 37 C.F.R. 3.73(b) statement (when there is an assignee)
10. ☐ English translation document (if applicable)
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
14. ☐ Certified copy of priority document(s) (if foreign priority is claimed)
15. ☐ Certificate of Mailing
☐ First Class ☐ Express Mail (Label No.: _____)
16. ☐ Small Entity statement(s) -- # submitted _____ (if Small Entity status claimed)

Accompanying Application (continued)

- 17.
- ☐
- Additional enclosures (please identify below):

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

<u>CLAIMS AS FILED</u>					
For	# Filed	# Allowed	# Extra	Rate	Fee
Total Claims	53	- 20 =	33	x \$18.00	\$594.00
Independent Claims	6	- 3 =	3	x \$78.00	\$234.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other Fees (specify purpose):					
BASIC FEE					\$690.00
TOTAL FILING FEE					\$1,518.00

☐ A check in the amount of _____ to cover the total filing fee is enclosed.☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.☒ Charge the amount of \$1,518.00 as filing fee.☒ Credit any overpayment.☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

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METHOD AND MATERIAL FOR REMOVING ETCH RESIDUE FROM HIGH ASPECT RATIO CONTACT SURFACES

FIELD OF THE INVENTION

5 The present invention relates to a novel method and material
for removing etch residue from high aspect ratio contacts, and more
specifically, to a process and material for cleaning contact opening surfaces
without substantially increasing the size or depth of the contact opening
and without producing a silicon rich oxide at the bottom of the contact
10 opening.

BACKGROUND OF THE INVENTION

One goal in forming many high aspect ratio (HAR) contacts
in integrated circuits is the deposition of a very thin layer of titanium at the
15 bottom of an etched opening, such as a via or trench. This layer facilitates
electrical contact between the contact material which will subsequently fill
the opening and the material to which it connects, *e.g.* doped polysilicon.
Prior to this deposition, an etching solution is utilized to form the
openings necessary in an insulative layer, for example, Boro-Phospho-
20 Silicate Glass (BPSG) or other insulator layer to provide the HAR contact
access to an exposed underlying conductive material. This conductive
material is usually formed of doped polysilicon, or some other conductive
substance. The thin titanium layer reacts with this polysilicon, usually in
the presence of heat, to form a titanium silicide layer.

Unfortunately, the materials used for etching the BPSG layer typically leave a polymer residue which ends up coating the inside and especially the bottom of the HAR contact opening. This residue must be removed before a titanium deposition can be initiated. The traditional way of removing this residue has been through the utilization of an oxygen (O_2) plasma strip step. The etch polymer residue reacts with the oxygen and is removed.

This process however, can leave behind a silicon rich oxide residue layer at the bottom of the opening because the oxygen also reacts with the polysilicon. The silicon rich layer can be represented as SiO_x , with x being between 0 and 2. This layer can also contain impurities, for example, carbon and fluorine impurities. This silicon rich oxide layer residue is substantially non-conductive, and therefore interferes with the deposition and of a conductive titanium material in the etched opening and the subsequent formation of a desirable titanium silicide layer at the bottom of the contact opening. This in turn affects the conductive performance of a conductor formed in the opening.

Traditional "wet chemistries" have been employed to remove the silicon rich oxide layer formed as a result of O_2 plasma stripping to further assist in preparing the HAR bottom surface opening for Ti deposition. However, these methodologies have not been entirely successful in removing the silicon rich oxide layer. These chemical methods are not generally selective to the silicon rich oxide layer, and thus they can

undesirably also etch the BPSG sidewalls of the opening and thereby increase its size.

What is therefore needed is an improved process for removing polymer etch residue from HAR contact openings which eliminates the formation of a silicon rich oxide layer within the contact opening. The process should also effectively eliminate the etch polymer from both the sides and bottom of the HAR opening without undesirably increasing its size.

SUMMARY OF THE INVENTION

The invention provides a method for removing etch residue from High Aspect Ratio openings, *e.g.* vias and trenches, in silicon wafer devices which involves contacting their surfaces with ammonia during at least a latter part of polymer residue removal. The method removes the polymer etch residue, without producing a silicon rich oxide layer within the contact opening and without substantially increasing the size of the contact opening. The invention permits the reliable deposition of a thin conductive layer, *e.g.* of titanium at the bottom of the contact opening, which can be used to form a silicide to improve the conductive performance of a conductor formed in the contact opening.

The invention also provides an integrated circuit having an ammonia-cleaned, polymer residue-free and silicon rich oxide-free high aspect ratio opening in an insulating layer.

5 The invention also provides a method of forming a contact opening in a semiconductor device which involves first etching a contact opening in an insulative layer in the device down to a polysilicon plug and then cleaning etch residue from the opening using ammonia gas.

10 Additional advantages and features of the present invention will become more readily apparent from the following detailed description and drawings which illustrate various embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross sectional view of a portion of an integrated circuit wafer in a intermediate stage of fabrication of a memory device.

15 Figure 2 is the wafer of Figure 1 having an insulative layer deposited thereon.

Figure 3 is the wafer of Figure 2 in which contact openings have been formed in the insulative layer.

20 Figure 4 is the wafer of Figure 3 showing etch residue in the contact openings.

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Figure 10A is a microphotograph representing an exposed side view of another contact opening bottom surface.

Figure 10B is a microphotograph representing an exposed side view of yet another bottom surface as a comparative example to Figure 10A.

Figure 10C is a microphotograph representing an exposed side view of still another bottom surface as a second comparative example to Figure 10A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention is directed to the removal of etch residue from contact openings or vias formed in semiconductor wafers. While all such contact openings or vias are contemplated herein, particular reference will be made to high aspect ratio (HAR) contact openings. As that term is used herein, "high aspect ratio" refers to aspect ratios from about 0.5:1 to about 20.0:1. Furthermore, reference shall also be made to the terms "wafer" and "substrate", which are to be understood as including silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) substrates, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. In addition, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions, junctions or layers in or over the base semiconductor structure or foundation. In addition, the semiconductor need not be

silicon-based, but could be based on silicon-germanium, germanium or gallium arsenide.

Referring now to the drawings in which like numerals indicate like components throughout the various embodiments, Figure 1 illustrates a portion of an integrated circuit wafer 10 at an intermediate stage of fabrication of a memory device. The integrated circuit wafer section 10 has a substrate 12. The substrate is formed of a material such as silicon. Field oxide regions 13, transistor gate stacks 15, doped regions 17 and capacitors 19 (illustrated as a single layer 19 but which actually contains a plurality of material layers as well know) are formed over the substrate. The substrate 12 also has conductive areas in the form of polysilicon "plugs" 14 formed thereon which have been deposited through a first layer of insulating material 16, which is usually a type of glass oxide well known in the art, for example, BPSG. The first layer of insulating material 16 may, in actuality, be formed as one or more layers of insulating material of, for example, BPSG.

Referring now to Figures 2 and 3, in the formation of HAR contact openings, a second layer of insulating material 18 is first deposited over the first layer 16. As shown in Figure 3, contact openings 20 are then formed through this second insulative layer 18 so as to contact the polysilicon conductive plugs 14. Openings 20 are formed through a patterned photoresist mask 21 which defines locations or areas to be etched, *i.e.* the openings. To form the HAR contact opening, an etchant is

applied to the insulating layer 18. Dry etching techniques known in the art are utilized for this purpose. Fluorine-containing gases, for example, are applied to the surface of the insulating layer 18 to form the opening 20. A non-exhaustive listing of such gases includes CH_2F_2 , CHF_3 , C_2F_6 , C_2HF_5 , and CH_3F , which may be used alone or in combination. After etching, the photoresist layer 21 is removed.

As shown in Figure 4, the etched opening 20 extends to the underlying plug 14. Unfortunately, after etching a polymer etch residue 22 is left in the opening 20, both on the sidewalls and the bottom of opening 20. This etch residue must be removed to enable a subsequent conductor placed in the opening to obtain good electrical contact with plug 14. Moreover, the deeper the opening 20, the more difficult it becomes to remove the etch residue 22 from the bottom thereof. Present attempts to remove this residue 22 typically involved an O_2 plasma etch, for example.

As shown in Figure 5, the O_2 plasma etch method has not proven entirely satisfactory, however. The oxygen plasma can remove the polymer residue 22, but in turn will form an undesirable layer 24 of a silicon rich oxide which can vary in depth over the bottom of the opening 20.

It is especially undesirable to have this oxidized layer 24 at the bottom of the HAR opening. This layer is relatively non-conductive and can interfere with both the deposition and the conductivity of a

subsequently-deposited thin conductive layer such as for example, titanium, which is used to form a silicide layer between a conductor material deposited in the opening and the underlying contact area, *e.g.* polysilicon. Since the underlying conductive area is typically formed of polysilicon, deposition of titanium coupled with a heat treatment yields a titanium silicide layer. The presence, however, of silicon rich residue can inhibit the formation of a desired layer of titanium silicide and leave an oxide rich material on the bottom of the contact opening which can interfere with subsequent processing steps during the contact fill process. The overall effect can significantly reduce conductivity, and affect device performance and yield.

The invention uses ammonia to remove the polymer etch residue. The use of ammonia to strip the polymer etch residue significantly reduces or eliminates oxidation of the HAR contact opening, thereby leaving a substantially oxide free side and bottom of the opening for the subsequent deposition of a conductive layer. Moreover, the use of ammonia does not substantially increase the size of the HAR opening, *i.e.* does not widen or deepen the opening as the reaction does not etch the BPSG sidewalls of the opening. As that term is used herein, "does not substantially increase" means an insignificant increase from an operational standpoint, for example, an increase of no more than a few Angstroms (\AA), *e.g.* about 5 Angstroms, more preferably about 1-2 Angstroms.

As used herein, "ammonia" refers to NH_3 in whatever form. Preferably, the ammonia will be in the form of a plasma, or as may be otherwise typically utilized in the art.

Operating parameters for the process of removing etch residue are set forth below. Preferably, the skilled artisan will find the use of an apparatus known in the industry as a Fusion Gemini Reactor useful for practicing the method of etch removal according to the various embodiments described herein. However, other apparatus are within the scope of the invention and will be similarly useful.

The ammonia should typically be applied at a temperature within the range of about 250 - 500° C. It is even more desirable to utilize temperatures within the range of about 300 - 400°C. Especially preferred is a temperature of about 350°C.

Operating pressure should be within the range of about .5 - 5 torr, and is most typically at about 1.5 torr. The applied wattage is usually within the range of about 500 - 5000 watts, with a range of about 1500 - 2000 watts being even more preferred. In many circumstances, 1900 watts will be especially desirable. A typical plasma coil can be utilized for providing the power necessary for the process of the invention.

The ammonia is applied to the HAR contact opening(s) at a rate within the range of about 100 to 4000 SCCM of NH_3 for a period of usually less than about 100 seconds. In a preferred embodiment, the time

of ammonia contact with the opening 20 can be about 75 seconds or less. The rate of application, time of operation and amount of NH_3 can vary somewhat according to particular operating conditions. Those skilled in the art may find that as the temperature goes up, the operating time can go down. Likewise, as the power is increased the time of operation may decrease as well.

Referring now to Figure 6, an exemplary embodiment of the process of the invention is illustrated: Using a fusion reactor 26, pressure is maintained at approximately 1.5 torr. The temperature of the reactor 26 is also set at about 350° . With an operating wattage of about 1900, NH_3 flows to the reaction chamber at a rate of about 750 SCCM, these conditions being sufficient to remove the etch residue 22. After no more than about 100 seconds, the NH_3 will have cleaned the polymer etch residue from the opening, while not substantially increasing its size. In addition, no silicon rich oxide is present at the bottom of the opening.

Figure 7 shows the same wafer 10 as shown in Figure 6 after the process of the invention has been completed. As can now be seen in Figure 7, the HAR contact opening 20 is clean of any polymer etch residue. At the same time, there is no significant increase in the size of the contact opening and no silicon rich oxide layer is present at the bottom of the contact opening. In this embodiment only NH_3 gas is used as the active gas to remove the polymer residue. A thin nitride layer 28 may be formed over the polysilicon plug 14.

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application of ammonia, with or without the preceding O₂ polymer etch removal step, will most typically yield a clean opening bottom surface without a silicon rich oxide layer thereon.

Referring now to Figure 8, following application of ammonia to remove the etch residue, and the optional step of wash chemistry to remove any remaining nitride layer, the HAR opening is now ready for application of a thin conductive layer of titanium (Ti) 31, which will form a silicide at the bottom of the contact opening 20, and subsequent steps to form a conductor 30 in contact with the bottom surface of the opening.

Titanium deposition in the contact opening 20 can be done in a manner known in the art. For example, titanium is deposited on the wafer using a sputter process commonly used with metals. A target containing titanium is surrounded by an argon plasma. Ions from the plasma hit the target surface. The titanium atoms which are removed from the metal target then coat the wafer surface. It is also possible to utilize CVD techniques in which the titanium is formed from the reaction of TiCl₄ with hydrogen (H₂). In any even, it is very important that the deposition material get down into the High Aspect Ratio opening, and reach the bottom surface of the opening or via 20. A collimator may be used to direct the atoms straight down, for better coverage on the contacts.

Titanium coats the inside of the contacts to improve the adhesion of a subsequently applied conductor plug 30, typically comprised

of tungsten, within the opening 20 of the insulative layer, *e.g.* BPSG. Following titanium deposition, there is a titanium anneal process which converts the titanium layer incontact with the polysilicon plug into Ti-silicide and possibly Ti-nitride. Single wafers are placed in a nitrogen
5 purged AG chamber, now more commonly known as a STEAG system for RTP (rapid thermal process). The chamber or system contains heat lamps which raise the temperature to within the range of about 700 - 750°C. As the temperature increases, the titanium reacts with polysilicon at the bottom surface in the contact opening 20 to form Ti-silicide. The titanium
10 may also react with the nitrogen in the chamber to produce Ti-nitride. Once annealed, the titanium is thus converted into two conductive material layers, Ti-silicide and Ti-nitride, which both reduce the contact resistance, with the Ti-nitride layer primarily acting as a silicon barrier during the tungsten deposition process. These layers will also help protect the silicon
15 substrate from being damaged by the subsequent tungsten deposition process.

The tungsten layer or "plug" provided in the HAR contact opening may be used, for example, to provide a conductive connection between metal runners and a memory cell in an integrated circuit.

20 A processing chamber can be used to deposit the tungsten onto the surfaces of the wafer, and into the HAR contact opening. This is typically a two-step process which uses tungsten hexafluoride (WF_6) and silane (SiH_4) to begin the tungsten deposition. The silane provides a

silicon source to tie up free fluorine atoms which can damage the substrate. After the initial layer of tungsten is produced, the deposition process is enhanced by replacing the silane with hydrogen gas. After tungsten "plug" deposition, the wafers may be rinsed and the integrated circuit is then ready for further fabrication according to methods known in the art. Figure 8 shows the device of Figure 7 in which a conductive plug 30 has been formed in the contact opening 20.

Referring now to Figures 9 - 10, there is presented actual microphotographs further illustrating the process of the invention, as compared with conventional O₂ stripping. The top two microphotographs in Figure 9 A represent high resolution exposed side views of a first contact opening bottom surface in a semiconductor device. The bottom two microphotographs Figure 9 A represent high resolution exposed side views of a second contact opening bottom surface. The top two and bottom two microphotographs in Figure 9 B represent high resolution exposed side views of a third and fourth contact opening bottom surface, respectively. The top two and bottom two microphotographs in Figure 9 C represent high resolution exposed side views of a fifth and sixth contact opening bottom surface, respectively. In Figure 9A, both the first and second contact opening bottom surfaces have been cleaned of polymer etch residue with ammonia only according to the process of the invention, followed by deposition of titanium, and subsequent deposition of a thin layer of titanium nitride followed by a layer of tungsten. In Figure 9B, a

comparative example, the third and fourth contact opening bottom surfaces have been cleaned of etch residue using conventional O₂ stripping with bias, followed by high temperature O₂ stripping with no bias. Following O₂ stripping, subsequent deposition of titanium and tungsten layers has occurred as in Figure 9A. Figure 9C, a second comparative example, the fifth and sixth contact opening bottom surfaces have been cleaned of etch residue using a high temperature O₂ strip with no bias. Following O₂ stripping, subsequent deposition of titanium and tungsten layers has occurred as in Figure 9A. In each of Figures 9A-C, the top left and bottom left microphotographs have been specially photographed to illuminate any oxygen present. The top right and bottom right microphotographs of each of Figures 9A-C have been specially photographed to show the presence of titanium and tungsten. In Figure 9A, which represents the process of the invention, both the top left and the bottom left microphotographs are dark, indicating that little or no oxygen is present in the first and second bottom opening contact surfaces. However, in both of Figures 9B and C, each of the top and bottom left photographs have a grainy white appearance at the bottom surface of each of the third through sixth contact openings, indicating the presence of a substantial amount of oxygen left over from stripping. In Figure 9A, the top and bottom right microphotographs are bold with clean lines, indicating the successful deposition of titanium in the first and second contact opening bottom surfaces. The thin band which can be observed across the top of the titanium silicide layer is the titanium nitride layer. In each of Figures 9B

and 9C, however, the deposited titanium and titanium nitride layers are much less pronounced with considerably more blurring. This indicates a less successful deposition on each of the third through sixth bottom surfaces, which is likely to have a negative impact on conductivity.

5 Figures 10A, 10 B and 10 C are high resolution microphotographs showing three additional contact opening bottom surfaces in side view close-ups. In Figure 10A, the contact opening bottom surface has been cleaned of polymer etch residue with ammonia only according to the process of the invention, followed by deposition of titanium, and subsequent deposition of a thin layer of tungsten. In Figure 10B, a comparative example, the contact opening bottom surface has been cleaned of etch residue using conventional O₂ stripping with bias, followed by high temperature O₂ stripping with no bias. Following O₂ stripping, subsequent deposition of titanium and tungsten has occurred as in Figure 10A. In Figure 10C, a second comparative example, the contact opening bottom surface has been cleaned of etch residue using a high temperature O₂ strip with no bias. Following O₂ stripping, subsequent deposition of titanium, titanium nitride and tungsten has occurred as in Figure 10A. As seen similarly with Figure 9A, Figure 10A shows a cleanly formed deposition layer of titanium, together with a well-defined thin band of tungsten across the top thereof. In contrast, both of Figures 10B and C present rather blurry, much less defined layers of titanium and tungsten, which is indicative of less successful depositions.

Although the invention has been described in connection with etching an opening or via for formation of a conductive plug, the invention can also be used to etch and subsequently etch-residue clean any opening, including, for example, openings used for form container capacitors in a memory circuit. Thus, the above description is only illustrative of exemplary embodiments which achieve the features and advantages of the present invention. It is not intended that the present invention be limited to these exemplary embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

What is claimed is:

1. A method for removing polymer etch residue from an etched opening in a silicon wafer device comprising contacting said opening with ammonia gas to remove said polymer etch residue.
2. The method of claim 1, wherein said opening is a High Aspect Ratio (HAR) contact opening.
3. The method of claim 2, wherein said contacting is performed under conditions effective to remove said etch residue without substantially increasing the size of said opening.
4. The method of claim 3, wherein said opening is contacted with ammonia gas in the absence of oxygen.
5. The method of claim 2, wherein said ammonia gas is in a plasma.

6. The method of claim 5, wherein said contacting is done at a temperature within the range of about 250 - 500° C.

7. The method of claim 6, wherein said contacting is performed in a plasma reactor within a power reactor range of about 500 - 2500 watts.

8. The method of claim 7, wherein said contacting is performed within a power range of about 1500 - 2000 watts.

9. The method of claim 7, wherein said contacting is performed with an ammonia gas flow rate within the range of about 500 to 1000 SCCM.

10. The method of claim 9, wherein said contacting is performed at power of about 1900 watts and a temperature of about 350°C.

11. The method of claim 10, wherein said contacting is performed with an ammonia gas flow rate of about 750 SCCM.

12. The method of claim 9, wherein said contacting is performed for a period of less than about 100 seconds.

13. The method of claim 12, wherein said contacting is performed for a period of not more than about 75 seconds.

14. The method of claim 1, further comprising forming a conductive layer at the bottom of said opening following said contacting step.

15. The method of claim 5, wherein said contacting step produces silicon nitride at the bottom of said opening, said method further comprising removing said silicon nitride.

16. A method for removing polymer etch residue from an etched opening in a silicon wafer device, comprising the steps of:

contacting said opening with an oxygen containing plasma, stopping said oxygen plasma contacting before said polymer etch residue is

completely removed and thereafter contacting said opening with ammonia gas.

17. The method of claim 16, wherein said contact opening is an High Aspect Ratio (HAR) opening, and said ammonia contacting step is performed under conditions effective to remove said etch residue without substantially increasing the size of said opening.

18. The method of claim 17, wherein said ammonia contacting occurs in the absence of oxygen.

19. The method of claim 18, wherein said ammonia gas is in a plasma.

20. The method of claim 19, wherein said ammonia contacting is performed at a temperature within the range of about 250 - 500° C.

22. The method of claim 20, wherein said ammonia contacting is performed at a temperature of about 350°C.

24. The method of claim 21, wherein said ammonia contacting is performed at a flow rate within the range of about 100 to 4000 SCCM.

26. The method of claim 25, wherein said bottom of said opening is not oxidized during said ammonia contacting step.

27. The method of claim 24, wherein said contacting is performed for a period of less than about 100 seconds.

28. The method of claim 27, wherein said contacting is performed for a period of not more than about 75 seconds.

29. A method of forming a contact opening in a semiconductor device, comprising:

- a) etching a contact opening in an insulative layer in said device down to a polysilicon element of said device; and
- b) cleaning etch residue from said etched opening by contacting said opening with ammonia gas.

30. The method of claim 29, wherein said contacting is performed under conditions effective to remove said etch residue without substantially increasing the size of said opening.

32. The method of claim 31, wherein said opening is contacted in the absence of added oxygen.

34. The method of claim 33, wherein said contacting is done in a plasma reactor at a temperature within the range of about 250 - 500° C, with a reactor power within the range of about 500 – 2500 watts, with an ammonia gas flow rate of about 500 to 1000 SCCM, and for a period of no more than 100 seconds.

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36.The method of claim 34, wherein said contacting is performed with a reactor power at about 1900 watts and a temperature of about 350°C.

37.The method of claim 34, wherein said contacting is performed with an ammonia gas at a flow rate of about 750 SCCM.

38.The method of claim 35, wherein said contacting is performed for a period of not more than about 75 seconds.

39.The method of claim 29, further comprising forming a silicide layer at the bottom of said contact opening following said contacting operation.

40.The method of claim 29, further comprising contacting said opening with an oxygen plasma between said etching and cleaning steps to remove a portion of said etch residue.

41. The method of claim 29, wherein an insulating layer is formed on said device prior to said etching and said etching forms a contact hole in said insulating layer.

42. The method of claim 41, wherein said etching is dry etching.

43. The method of claim 42, wherein said dry etching is performed using at least one fluorine-containing gas.

44. The method of claim 43, wherein said fluorine-containing gas is at least one gas selected from the group consisting of CH_2F_2 , CHF_3 , C_2F_6 , C_2HF_5 , and CH_3F .

45. A semiconductor device comprising:

an insulating layer; and

an ammonia-cleaned etched opening in said insulating layer;

and,

a conductor formed in said cleaned opening.

46. An integrated circuit comprising an ammonia-cleaned, etch residue-free High Aspect Ratio opening provided in an insulating layer, said opening being formed atop a polysilicon region, said opening containing a conductor which electrically connects with said polysilicon region.

47. An integrated circuit as in claim 46 further comprising:

a silicide layer between said conductor and said polysilicon region.

48. An integrated circuit as in claim 46, wherein said integrated circuit is a memory circuit.

49. An integrated circuit as in claim 47 wherein the interface area between said conductor and polysilicon region is free of oxygen contamination.

50. A method of forming an integrated circuit structure comprising:

forming an insulating layer over a polysilicon region;

forming a high aspect ratio contact opening in said insulating layer down to said polysilicon region using a fluorine containing gas;

removing polymer residue from said contact opening using a gas which provides an oxide free bottom of said contact opening;

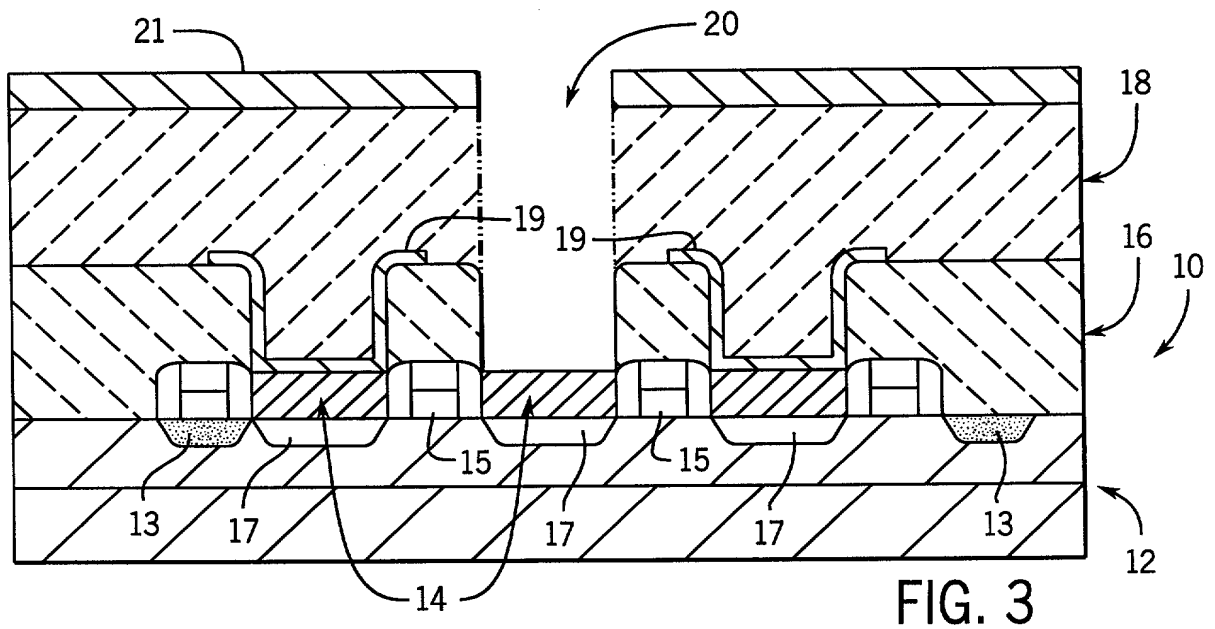
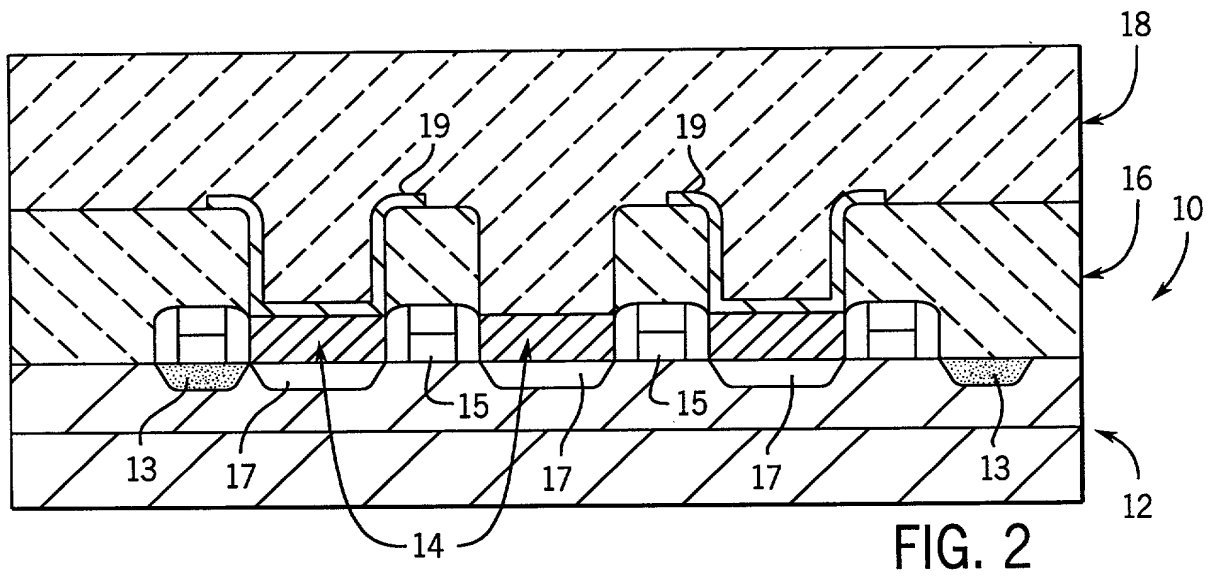
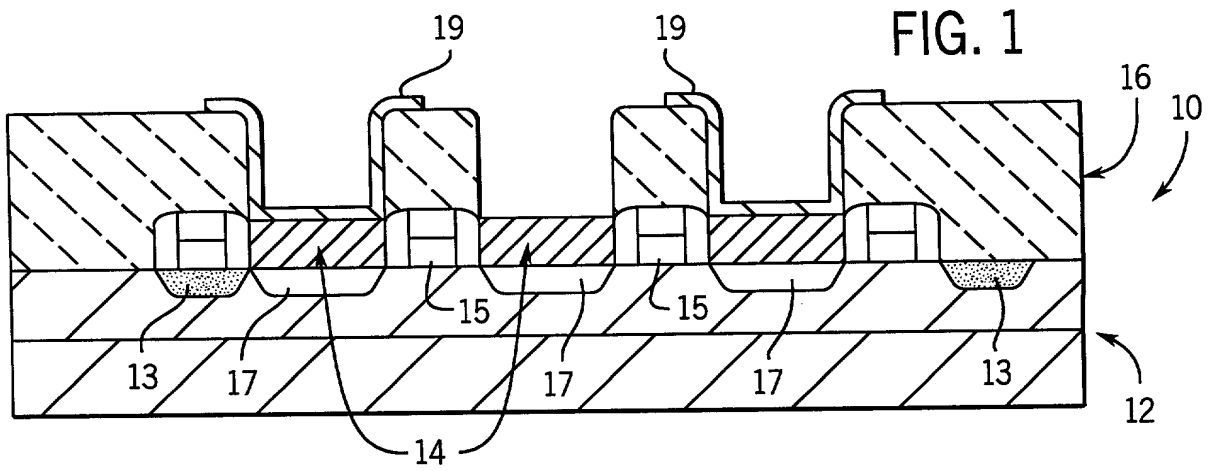
forming a silicide layer at the bottom of said opening in contact with said polysilicon layer;

forming a conductor in said opening in electrical contact with said silicide layer.

51. A method as in claim 50 wherein said gas for removing said polymer residue is ammonia gas.

52. A method as in claim 50 further comprising removing a portion of said polymer residue from said contact opening with oxygen prior to using said gas which provides an oxide free bottom of said contact opening.

53. A method as in claim 50 wherein said silicide layer is a titanium silicide layer.



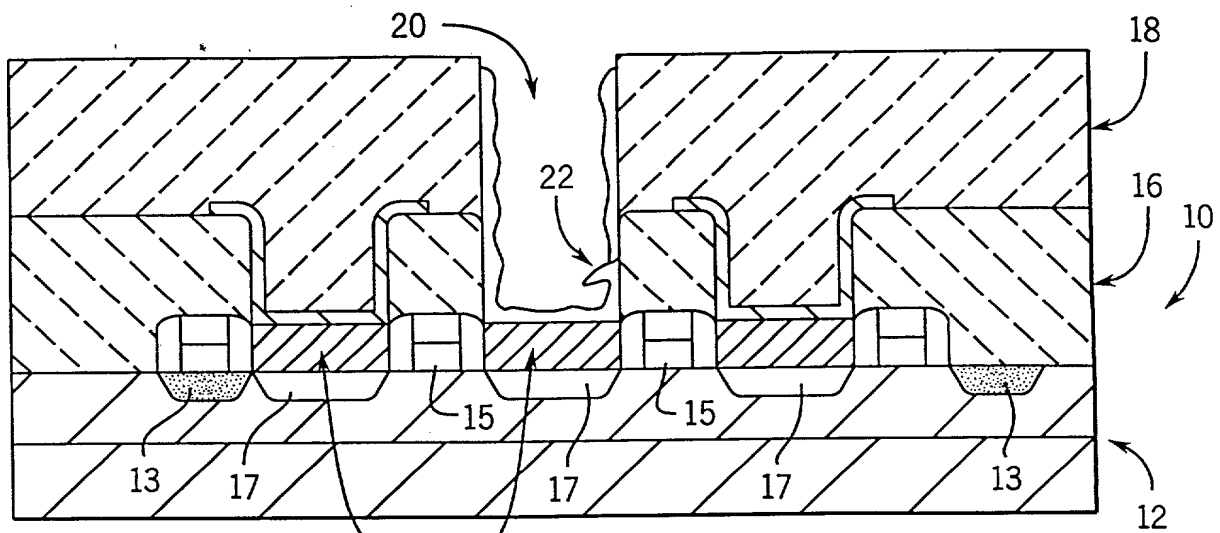


FIG. 4

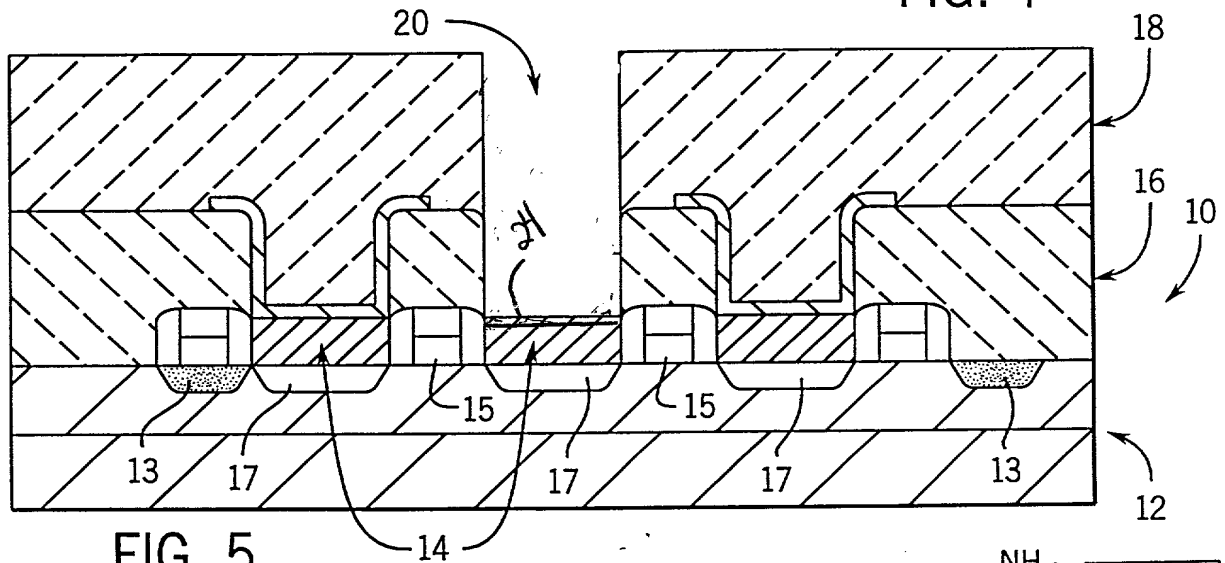


FIG. 5

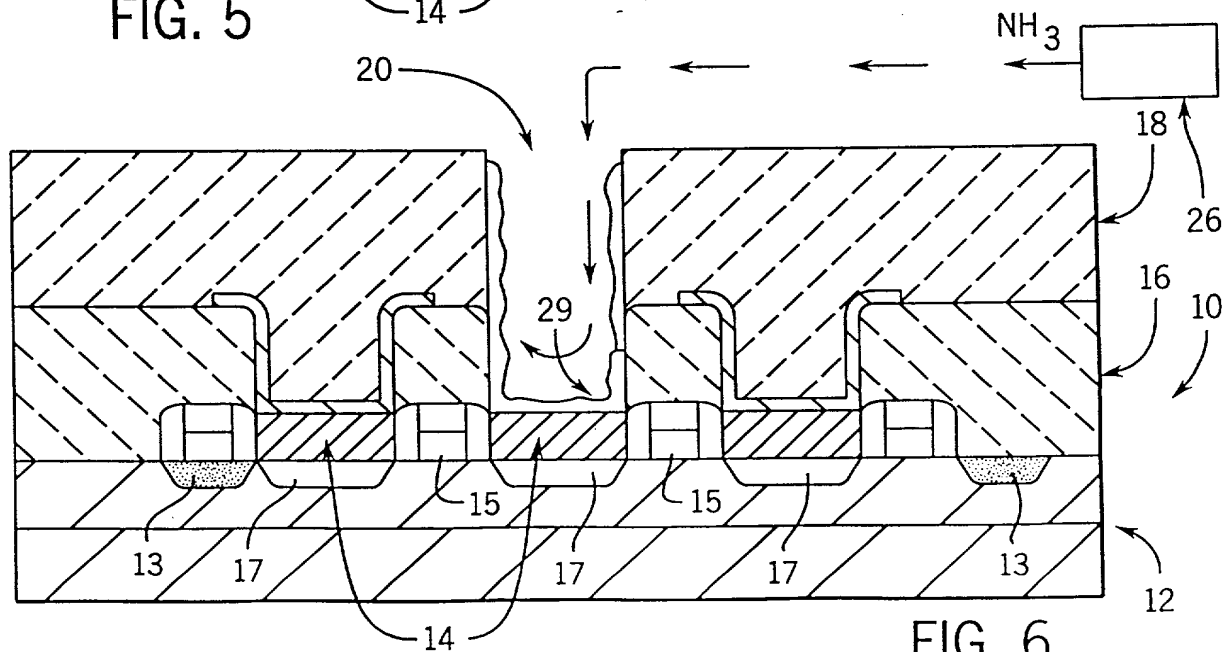


FIG. 6

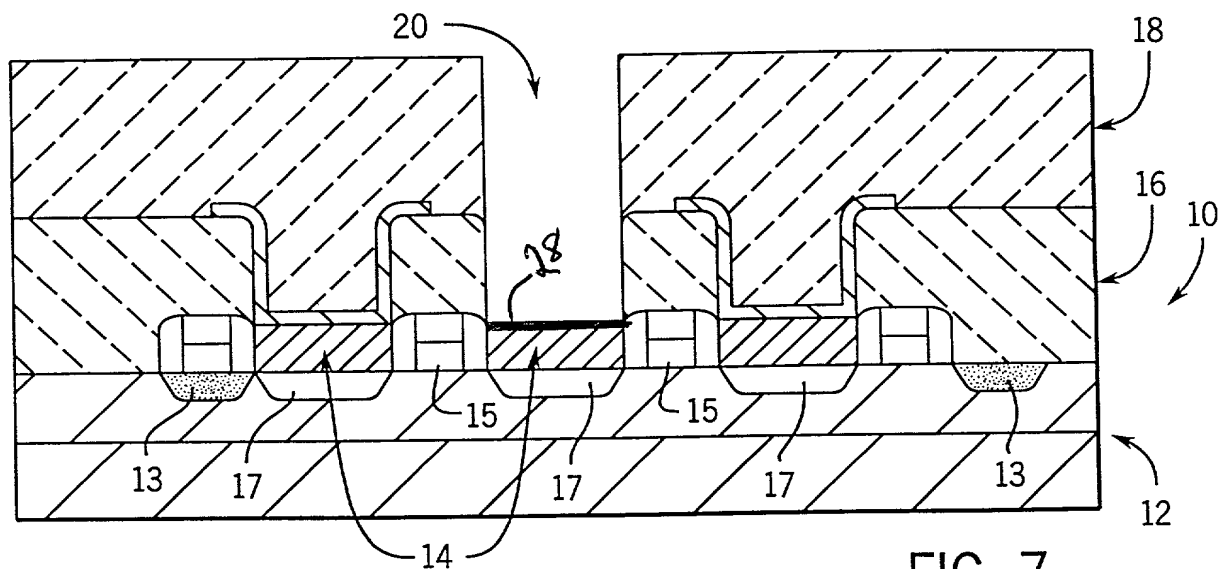


FIG. 7

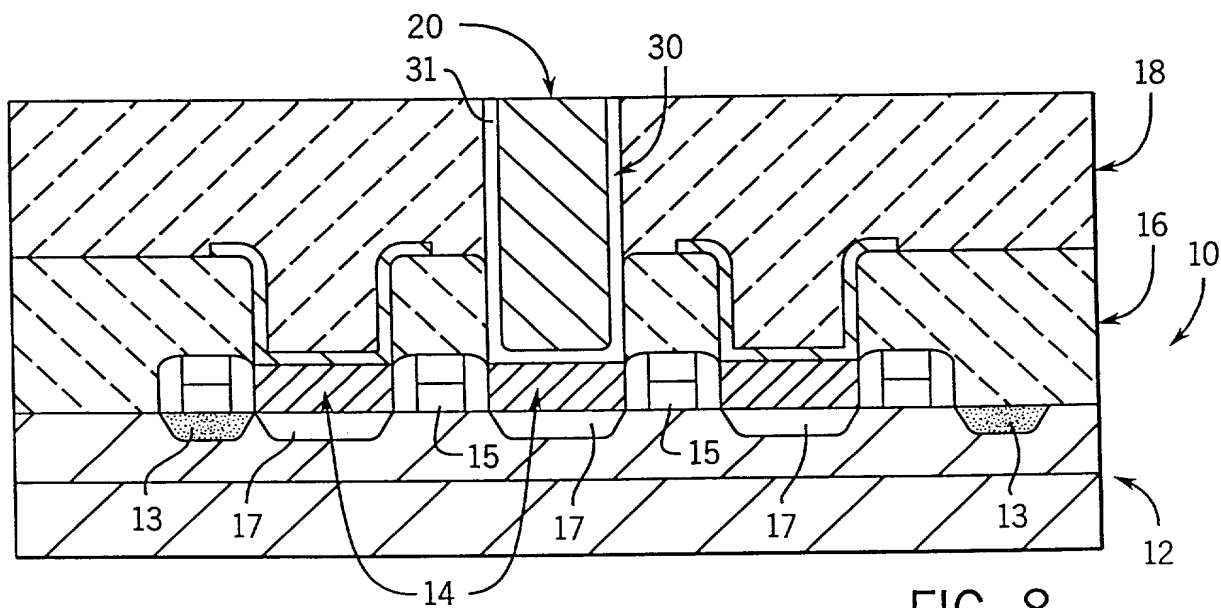


FIG. 8

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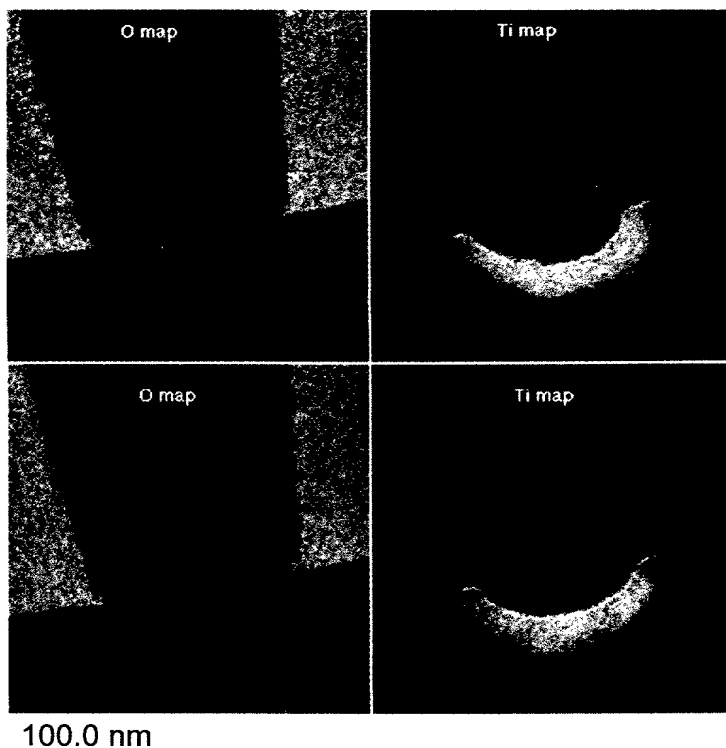


FIG. 9A

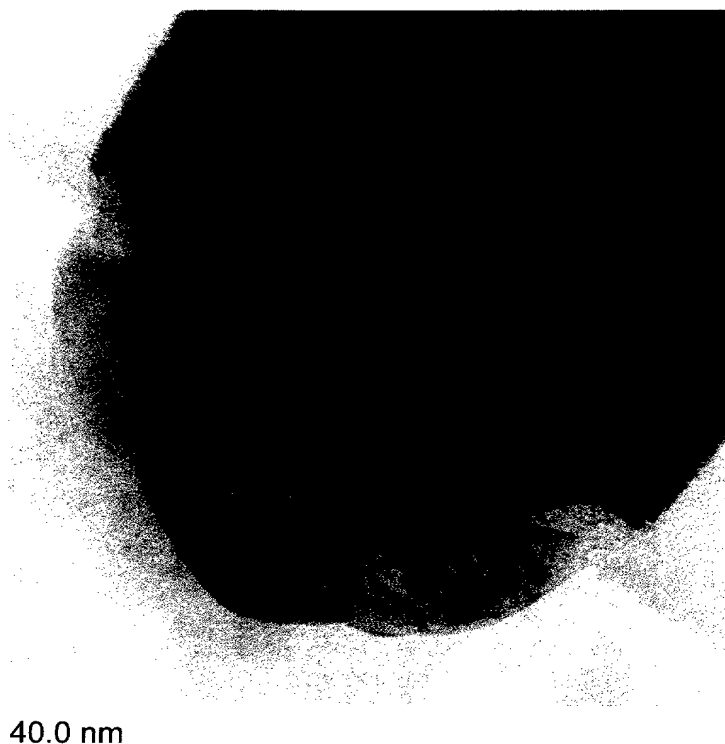
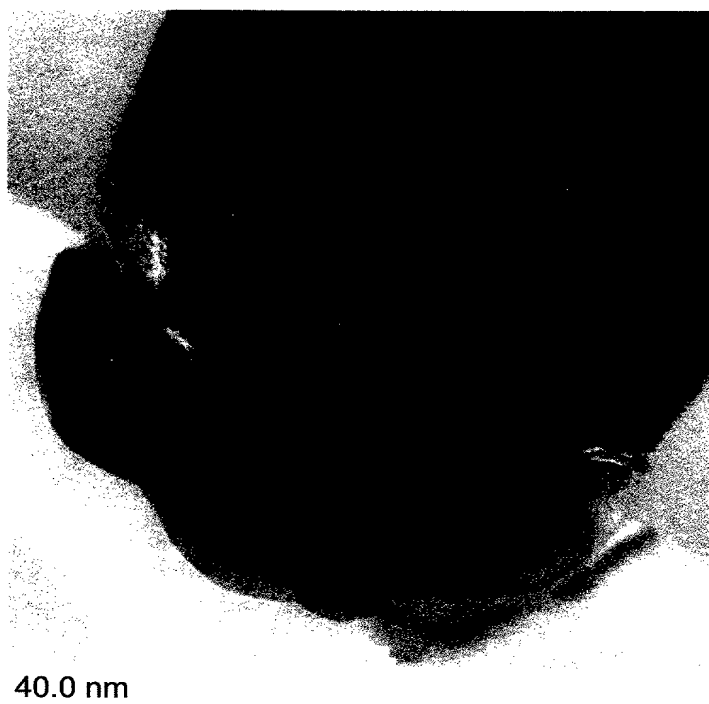
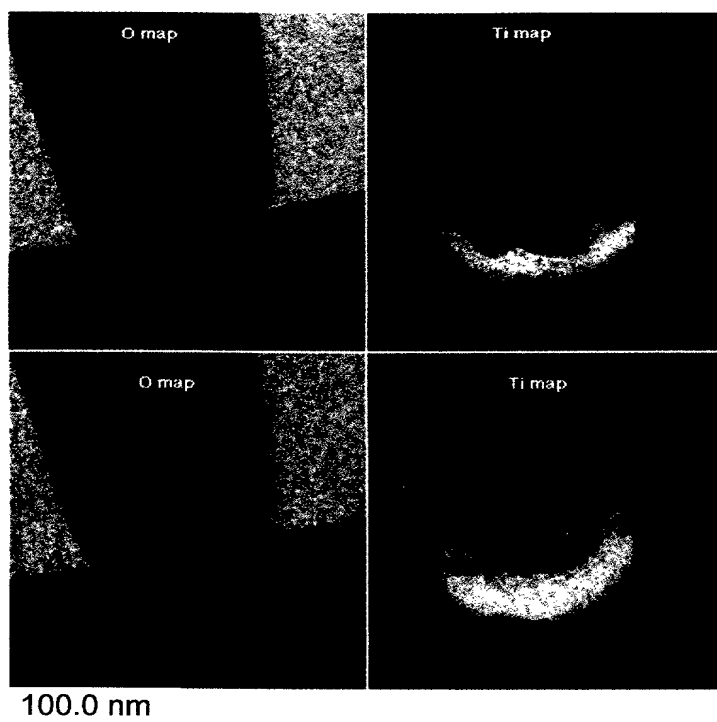


FIG. 10A



Docket No.: M4065.0239/P239

Micron No.: 99-0544.00/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND MATERIAL FOR REMOVING ETCH RESIDUE
FROM HIGH ASPECT RATIO CONTACT SURFACES

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

NONE

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

NONE

Docket No.: M4065.0239/P239
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
DECLARATION FOR PATENT APPLICATION

Signature Page for Second Inventor

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Steve Byrne

Date:

8-31-00

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Docket No.: M4065.0239/P239

Micron No.: 99-0544.00/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

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